AN INCREMENTAL ANALOG-TO-DIGITAL CONVERTER

A THESIS

Presented to

the Faculty of the Graduate Division

by

Frank Robert Williamson, Jr.

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

Georgia Institute of Technology

June, 1961

42
12-L

AN INCREMENTAL

ANALOG-TO-DIGITAL CONVERTER

Approved

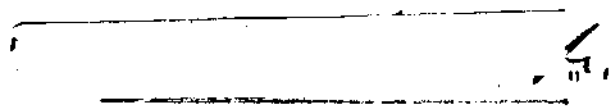
W. B. Jones, Jr.

Robert S. Johnson

Joseph L. Hammond, Jr.

Date approved by chairman May 18, 1961

"In presenting the dissertation as a partial fulfillment of the requirements for an advanced degree from the Georgia Institute of Technology, I agree that the Library of the Institution shall make it available for inspection and circulation in accordance with its regulations governing materials of this type. I agree that permission to copy from, or to publish from, this dissertation may be granted by the professor under whose direction it was written, or, in his absence, by the dean of the Graduate Division when such copying or publication is solely for scholarly purposes and does not involve potential financial gain. It is understood that any copying from, or publication of, this dissertation which involves potential financial gain will not be allowed without written permission.



ACKNOWLEDGMENTS

The author wishes to express his sincere appreciation for the valuable criticisms and guidance given by Doctor William B. Jones, Jr. (Thesis Advisor) and Robert S. Johnson and Joseph L. Hammond, Jr. (members of the Reading Committee).

The material for this study is taken from the work done by the author on the sponsored project A-497 (contract number DA-01-009-ORD-853) conducted at the Georgia Tech Engineering Experiment Station. This project was concerned with the investigation and development of a method of conversion which would result in a less expensive analog-to-digital converter than those currently available for use with the TRICE computer.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

SUMMARY

This thesis describes the design, construction, and evaluation of a high speed incremental analog-to-digital converter. This converter is to be used to connect a general purpose analog computer to a special purpose digital computer named the TRICE which was recently developed. The purpose of the analog-to-digital converter constructed for this study was to evaluate a method of conversion that could yield a unit less expensive and complex than existing methods. It was required that the converter developed retain sufficient accuracy and repeatability to be competitive with devices currently available for this application.

The converter is developed on the principle of a closed loop circuit with a digital-to-analog converter contained in the feedback path. The forward path of the circuit has the capability of adjusting the digital output until the difference between the unknown input voltage and the output of the digital-to-analog converter is reduced to a minimum. When this difference is at a minimum, the digital value at the output of the analog-to-digital converter represents the value of the unknown voltage at the input.

For the application described above, the digital output of the converter is to be an incremental representation of the voltage at its input. This incremental digital representation may be given the form of a train of positive and negative pulses where each pulse represents a change of a fixed increment in the input voltage to the converter. The summation of these pulses will give the value of the unknown voltage at

the input of the converter. By causing these pulses to have an equal volt-second area, this summation may be done by integration and the digital-to-analog conversion may be done by an electronic analog integrator. The use of the form of the incremental digital signal described above and the analog computing technique for the digital-to-analog converter in the feedback path gives a simplification in the design and complexity of the analog-to-digital converter over present methods.

The results of the evaluation of the converter constructed for this study are presented in the text of this thesis and indicate that the conversion method used here allows a converter to be built to meet the desired specifications. These include an input voltage range of plus 100 volts to minus 100 volts and a bit size adjustable over the range of 100 millivolts to 10 millivolts. A conversion accuracy and repeatability of 0.1 percent of full scale was achieved for a maximum conversion rate of approximately 15,000 bits per second.

CHAPTER I

INTRODUCTION

The analog-to-digital converter is a device that converts an analog or continuous representation of a variable quantity into an equivalent digital representation. If the analog quantity is a problem variable of an analog computer, the analog-to-digital converter may be used to change this variable into a form that is acceptable by a digital computer. This ability to transfer the problem variables of the analog computer to the digital computer may be used to an advantage in certain applications. These applications include such areas as data processing or problem solution where the data may exist in an analog form.

The purpose of this study is to evaluate a method of analog-to-digital conversion and to discuss the development of a converter based on this method. This analog-to-digital converter is to be used to connect a general purpose analog computer to the TRICE, an incremental digital computer recently developed by Packard-Bell Electronics Corporation. The converter will be used to continuously monitor an output variable of the analog computer and to convert this analog information into a suitable digital form for acceptance by the digital computer.

The converter discussed here differs from previous conversion methods through the use of analog techniques for a major part of the system. A simplification in the design is obtained through the elimination of the customary digital register by the substitution of an analog storage using an operational amplifier as an integrator.

CHAPTER II

BACKGROUND

Early techniques.--The need for analog-to-digital converters arises out of the fast-advancing state of the art of analog and digital computers. Many techniques for converting voltages into digital numbers have been presented. These included mechanical, electrical-mechanical, and electronic principles. H. E. Burke cited in a survey on analog-to-digital converters in 1953 that there were over one hundred different devices that had been demonstrated in breadboard form in the three years previous.[1] The majority of these converters did not contain feedback. Typical examples of these converters are the fixed-interval device using a variable frequency oscillator and the chronometric technique using a ramp or phase device.

The chronometric technique using a ramp generator is used in some low-speed electronic analog-to-digital converters presently on the market.[2] This is a good example of a conversion method not employing feedback. A linearly-rising voltage ramp is compared with the unknown voltage to be measured. The linear voltage ramp allows time to be the actual variable used in the measurement. Coincident with the start of the ramp, a gate on an accurate oscillator is opened so that pulses from the

---

[1]H. E. Burke, "A Survey on Analog-to-digital Converters," Proceedings of the Institute of Radio Engineers, Vol. 41, August 1953, pp. 1455-1462.

[2]Albert S. Jackson, Analog Computation, New York, McGraw-Hill, 1960, pp. 562-563.

oscillator appear at the input of an electronic counter circuit. These pulses are counted until the magnitude of the ramp is equal to that of the unknown voltage at the input of the converter. By proper scaling of the frequency of the oscillator and the slope of the voltage ramp, the bit size or converter resolution may be adjusted. The number contained in the counter at the end of the conversion represents the unknown voltage. When the next conversion is to be made, the ramp is reset to its original value and the counter is reset to zero. The time necessary for conversion is dependent upon the input voltage. This converter is limited in conversion speed and resolution due to the maximum counting rate of the electronic counter. A limitation on accuracy and linearity of the conversion is the precision with which the ramp may be generated.

Feedback converters.--The application of feedback methods to analog-to-digital converters was described in 1953 by B. D. Smith.[3] Feedback as applied to converters may introduce several advantages such as a decrease in the time necessary for conversion and an increase in the accuracy of the conversions. The basic consideration introduced by Smith was the use of a digital-to-analog converter or "decoder" in the feedback circuit of the analog-to-digital converter.

Consider a digital-to-analog converter which contains a network composed of resistors and current or voltage sources that may be switched on or off by external signals. The effect produced by the sources at the output of the network may have equal weight or may be weighted according to some numerical base such as the binary number system. The theorem of

---

[3]B. D. Smith, "Coding by Feedback Methods," Proceedings of the Institute of Radio Engineers, Vol. 41, August 1953, pp. 1053-1058.

superposition allows us to consider the network as some equivalent circuit whose open-circuit voltage, short-circuit current, or voltage or current into a constant load resistance will be a summation of the effects of all of the sources. Thus, the output analog value will be a function of the state of the signals controlling each source and the function by which each source is weighted. The control signal for each source may be derived from a digital register in which the digital value is entered for decoding or conversion. The output analog value of the network is controlled by the register and represents the digital value in the register of the digital-to-analog converter.

The analog-to-digital converter using feedback makes a comparison between the output of a digital-to-analog converter and the unknown analog voltage.[4] This comparison is made at the input of a high gain amplifier. The polarity of the voltage at the output of the amplifier tells if the output of the digital-to-analog converter is above or below the value of the unknown input voltage. This information may be used to direct a change in the output of the digital-to-analog converter in a manner to reduce the differences between the two voltages at the input of the comparing amplifier. If the digital-to-analog converter is of the form described above, reducing the difference of the voltages at the input of the amplifier will bring the digital value contained in the register to the value of the unknown input voltage.

The converter described above using feedback may have the advantage of greater conversion speed, accuracy, and resolution over non-feedback techniques such as the chronometric technique using a ramp

---

[4]Jackson, op. cit., pp. 563-564.

generator. This is due to the ability of the digital-to-analog converter to be coded so that each decision may have a different weight on the total. The value desired may then be reached with fewer decisions or operations. The increased complexity of the analog-to-digital converter using feedback gives non-feedback methods some advantage in cost and circuit simplicity.

Coding techniques.--The method in which the output of the digital converter approaches the unknown analog is directed by a control section contained in the analog-to-digital converter. There are two methods that are of particular interest and will be discussed here. The first of these two methods uses a forward-backward counter or bidirectional counter.[5] This responds to changes in the analog input by counting in the direction of the change in the unknown input voltage. As the counting proceeds, the feedback voltage changes with each count by an increment equal to the least significant bit or change that may be produced at the output of the decoder. The changes in the output of the decoder are in the direction that causes a reduction in the difference between the value of the unknown input voltage to the converter and the digital representation of this voltage at its output. If the input voltage does not exceed the bandwidth of the converter, the value contained in the digital counter will be the value of the input voltage. The digital counter is capable of a minimum change equal to the least significant bit which will produce an error at the output of the converter no greater than the amount represented by this least significant bit. This method of conversion shall be refered to as incremental conversion.

The second method in which a converter may approach its final value

---

[5] Ibid., pp. 564-565.

is best described by considering the illustration of a pure binary coder. The effect of each decision or operation at the output of the digital-to-analog converter contained in the feedback path is weighted according to the binary number system.[6] Any bit being considered has a value equal to the sum of all less significant bits plus the value of the least significant bit. If a unilateral converter is considered for the illustration where the input will always be of the same polarity, the register and the output of the decoder may be set to zero for each conversion. The first comparison is made by switching on the largest bit so that the voltage at the output of the digital-to-analog converter rises from zero to half of its full scale value. If the unknown input voltage is less than this value, the bit is switched off and a zero is entered in this position in the register. If the value is less than the input voltage then the bit is left on and a one is entered in this position. The next most significant bit is then switched on and the comparison is made as before. The comparisons are then made for each bit separately in the order of decreasing magnitude until the smallest bit is decided. At this time the conversion is complete and the value of the output of the decoder is within plus or minus the magnitude of the least significant bit of the unknown input voltage. The digital register then contains the value of the input voltage. This method is called the ripple-down method.

The use of the feedback in the ripple-down converter allows the decoder to be programmed so that the number of decisions necessary for a conversion is reduced and the conversion rate is increased. The

---

[6]Ibid., pp. 565-566.

ripple-down converter makes an independent conversion of the value of the unknown voltage for each conversion period. This method is not limited to the binary number system.

Delta modulation.--A modulation system invented in Europe is discussed here because its operation is similar to that used to solve the problem in this study.[7] This system produces a series of positive and negative pulses whose sum is proportional to the time varying voltage at the input. This system is illustrated in the block diagram in Figure 1. The similarity of this system to the incremental converter discussed in this study is the pulse output description of the input voltage and the manner in which feedback is used to detect changes in the input voltage. The output pulse train is an incremental digital representation of the changing voltage at the input to the modulator.

This system is not adequate for the intended application of the analog-to-digital converter being developed here due to the finite time constant of the lowpass filter used in the feedback path of the modulator. A comparator circuit looks at the difference between the input voltage and the output of a lowpass filter. The error voltage is introduced into the pulse generator and when this voltage exceeds a predetermined level, a pulse is generated. The polarity of this pulse is chosen to reduce the difference between the input voltage and the output of the lowpass filter. The lowpass filter has a long time constant compared to the duration of the pulses so that its output changes by fixed steps with the input pulses. The lowpass filter located at the transmitter is identical

---

[7]F. K. Bowers, "What Use is Delta Modulation to the Transmission Engineer?" Transactions of the American Institute of Electrical Engineers, Vol. 78, 1957, pp. 142-147.

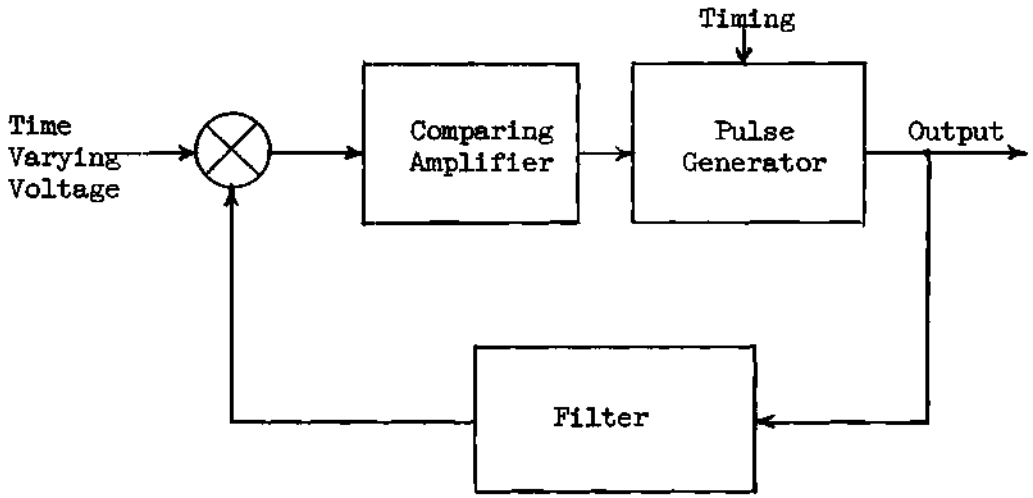


Figure 1. Block Diagram of Delta Modulation System

with the one contained in the receiver. When the pulses are reshaped at the receiver and applied to the input of the filter, the filter output reproduces the feedback voltage to the comparator at the transmitter. The error necessary to generate a pulse at the transmitter may be known and determines the resolution of the system. This modulation technique is known as Delta Modulation.

CHAPTER III

DESIGN OF THE CONVERTER

Design Philosophy

Incremental conversion.--The analog-to-digital converter developed in this thesis uses the coding technique defined in the previous chapter as incremental conversion. The digital output of this converter follows the changes in the input voltage by advancing in the direction of these changes by increments equal to the least significant bit contained in the digital register of the converter. The changes in the unknown input voltage may be followed by observing the direction and rate of the corresponding changes in the digital output of the converter. This incremental information may be represented by a series of positive and negative pulses. Each pulse represents a change of one increment in the input voltage to the converter. The direction of the change at the input may be represented by the polarity of the pulse describing the change. An incremental digital representation of this form is shown in Figure 2.

The incremental digital form introduced above may be considered equivalent to the coding of the derivative of the input voltage. This view is taken from the fact that each pulse at the output of the converter represents a change of a fixed amount in the input voltage to the converter. The rate of these output pulses represent the derivative or rate of change of the unknown input voltage.

Incremental digital-to-analog converter.--The digital-to-analog converter accepts as its input a digital representation of some voltage and presents

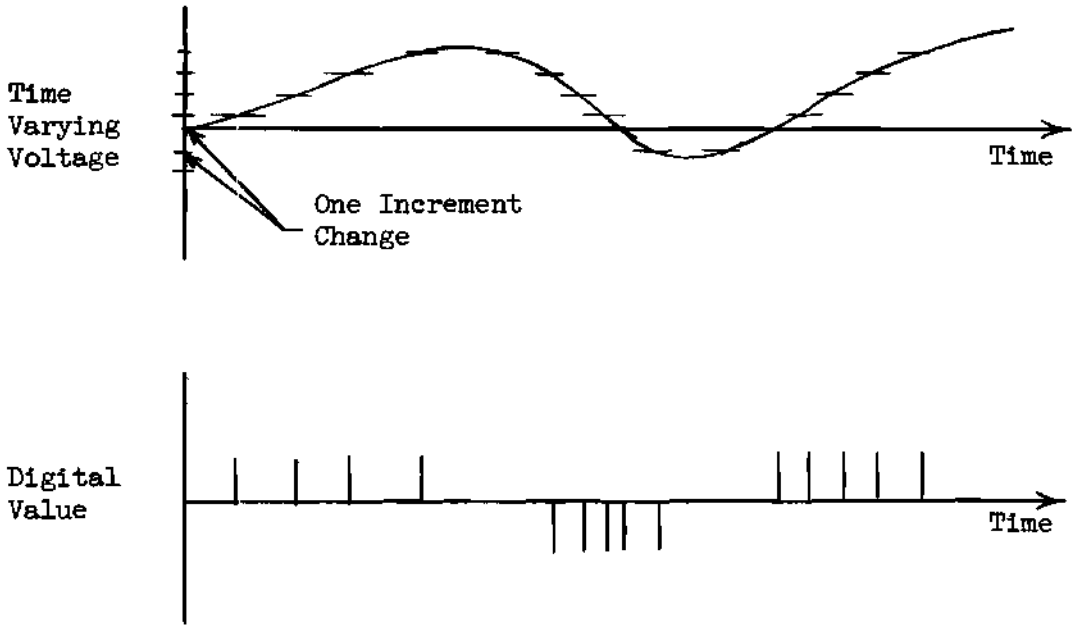


Figure 2. An Incremental Digital Representation of a Time Varying Voltage

this value in analog form as its output. The digital-to-analog converter used here will accept the incremental digital form described above. The output is a voltage that changes by a fixed amount with each input pulse. To obtain the value of voltage represented by the incremental digital signal, it is necessary to store (sum or integrate) all of these incremental changes. This storage could be implemented by use of a counter capable of adding the positive pulses and subtracting the negative pulses from the number contained in the counter. The conversion to the analog form would then be made by a suitable network controlled by this counter. This type of digital-to-analog converter is discussed in the previous chapter.

If the incremental digital signal is represented by pulses of equal volt-second area, then the analog conversion may be accomplished by time-integration of the pulse train. A suitable electronic integrator is shown in Figure 3. This circuit comprises an operational amplifier with capacitive feedback, forming a precision Miller integrator.

The output of this integrator changes by a fixed amount with each incoming pulse. Thus, the output voltage is proportional to the sum of all input pulses. This approach yields a converter which is less expensive and less complex than conventional devices, but retains adequate accuracy and resolution. For this reason, the pulse-integration technique was adopted for the digital-to-analog converter required in this thesis program.

Incremental analog-to-digital converter.--The analog-to-digital converter developed here is a closed-loop device built around a digital-to-analog converter in the manner described in Chapter II. The digital-to-analog converter illustrated in Figure 3 is used in the feedback path of the

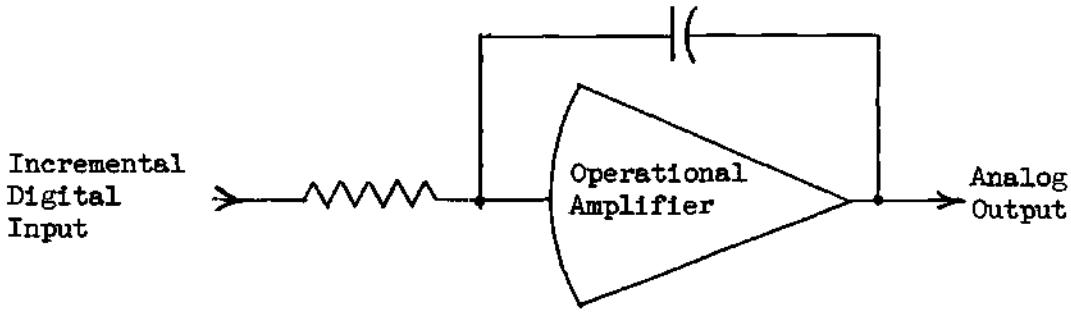


Figure 3. Incremental Digital-to-analog Converter

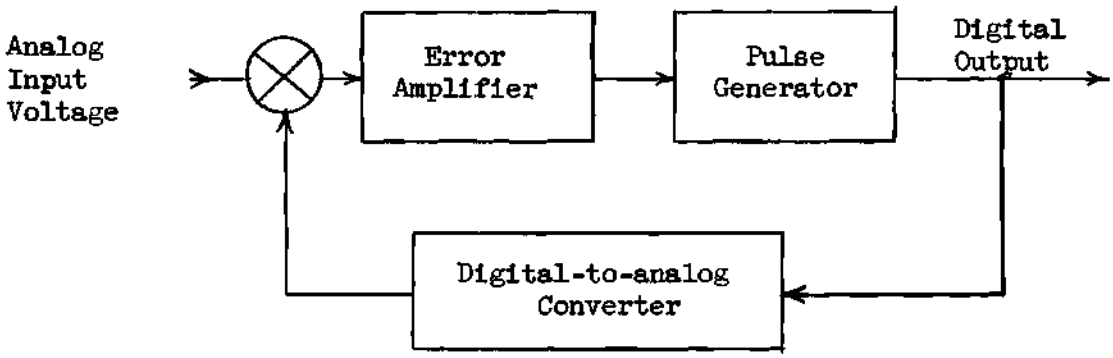


Figure 4. A Simplified Block Diagram of the Analog-to-digital Converter

analog-to-digital converter. The unknown input voltage is summed with the output of the digital-to-analog converter in an analog program that provides information on the difference of the two voltages. A simplified block diagram is illustrated in Figure 4. When the magnitude reaches a predetermined level, a pulse appears at the output of the Pulse Generator. The polarity of this pulse is chosen to reduce the difference between the unknown input voltage and the output of the digital-to-analog converter. The error magnitude at which a pulse is generated is chosen so as to keep the output of the digital-to-analog converter within one incremental bit of the input voltage to the converter.

The application of the incremental analog-to-digital converter discussed here requires that it operate synchronously with timing pulses from the digital computer. The Packard-Bell TRICE computer uses a repetitive word consisting of a 30-bit serial code. The converter information must be available at the proper time in the serial code for the digital computer to accept the information. The converter is synchronized to the TRICE word rate by means of accurately determined timing pulses from the digital computer. The synchronous operation of the converter will create a condition in which the magnitude of the error voltage may exceed the limit set for a one-bit change between two timing pulses. This is due to the inability of the Pulse Generator to generate a pulse until the next timing signal from the computer. The effect of this condition is illustrated in Figure 5.

Input Signal and Converter Parameters

The specifications imposed on the design of the analog-to-digital converter are the following. The limits of the input voltage range of

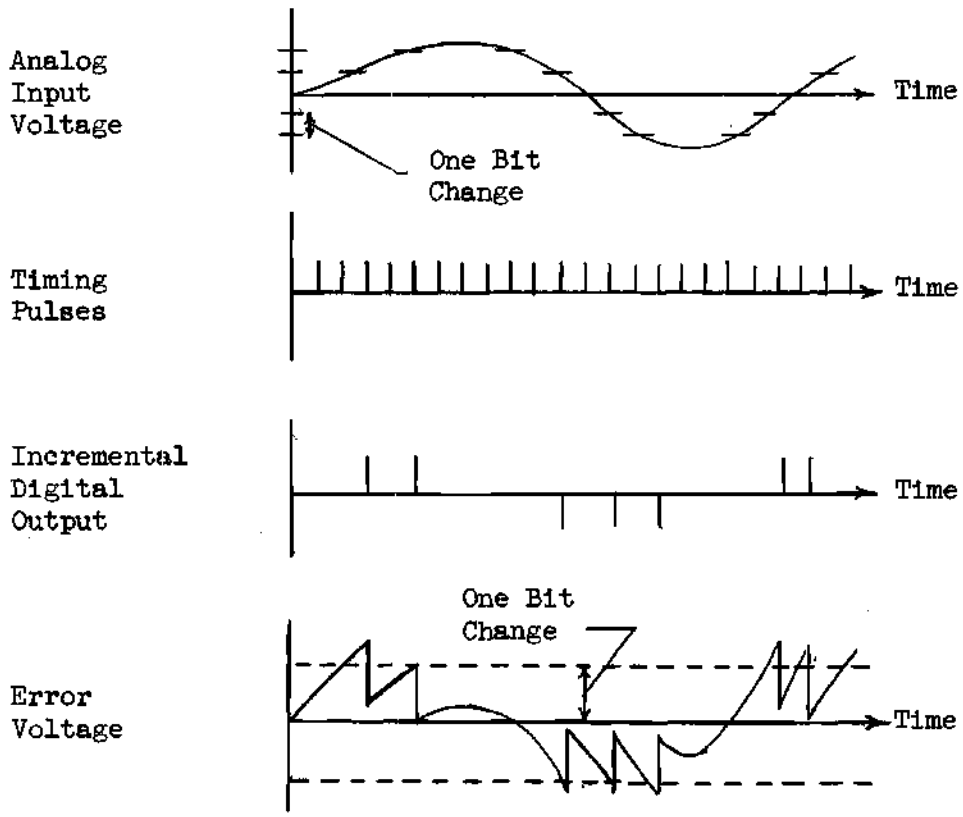


Figure 5. Typical Waveforms for Synchronous Operation of the Analog-to-digital Converter

the converter are plus and minus 100 volts. The bit or increment size should be adjustable over the range of 10 millivolts to 100 millivolts. Accuracy and repeatability of the conversions should be equal to or better than 0.1 percent of full scale.

For compatibility with the TRICE, the incremental digital output of the analog-to-digital converter should be in the form of a two-bit binary parallel code. This form of the incremental digital signal is presented at the digital output of the converter simultaneously with the incremental pulse description at the input of the digital-to-analog converter. One of the parallel code outputs indicates in a binary form the existence or non-existence of an incremental change in the voltage at the input of the converter. The second digital output for the parallel code indicates in a binary form the sign of the incremental change that has occurred. This digital form is a two-bit binary parallel code. A negative eight-volt level at the Bit Output indicates the existence of an incremental change and a negative eight-volt level at the Sign Output indicates that the increment was negative. Zero volts at the Sign Output indicates a positive incremental change if a change was indicated at the Bit Output. Zero volts at the Bit Output signifies the non-existence of an incremental change.

Two timing pulses are available on separate inputs from the digital computer. These input pulses are designated as the P_3 pulse and the P_{30} pulse, where the subscript denotes the position in the 30-bit serial code word. Thus, the P_3 pulse occurs simultaneously with the third bit in the computer word and the P_{30} pulse occurs at the end of the computer word. With a computer word rate of 100,000 words per second, the P_3

pulse follows the P_{30} pulse by 0.9 microseconds. It is during the 9.1-microsecond period between the P_3 pulse and the P_{30} pulse that the incremental digital information is to be available from the converter. The output information during this period describes the condition existing at the last P_{30} pulse.

The maximum conversion rate possibly required of the converter is 100,000 conversions per second, which is equal to the word rate of the TRICE computer in words per second. The operational-amplifier step response and other practical considerations suggest an upper limit on the conversion rate of about 10,000 bits per second.

Berkeley Model 1048 chopper-stabilized operational amplifiers were used in the subject system. For the increment sizes given above, higher bit rates are limited due to the necessary increase in the gain of the integrator serving as the digital-to-analog converter. This increase in gain is necessary in order to keep the equivalent area of the pulses constant. The high gain introduces errors in the conversions through an increased drift in the voltage stored on the feedback capacitor.

If the conversion or bit rate is limited to a value less than 100,000 bits per second, the timing pulses described above are divided down so that the equivalent word length of the converter includes an integral number of computer words. This gives the appropriate time scaling for the converter and introduces a scale factor into the conversions due to the digital output information from the converter being displayed through more than one word length on the TRICE computer. This number is a known constant for any selected division of the timing pulses. The division of the timing pulses is accomplished through the use of binary counters. This division is done external to the converter.

Circuit Description

Basic Divisions.--A complete block diagram of the analog-to-digital converter designed in this thesis is shown in Figure 6. This block diagram is divided into seven basic sections, which are indicated by the dashed lines separating each section. These sections are made according to the function of the enclosed circuit and are discussed in detail. The details of the circuits illustrated in the block diagram in Figure 6 are shown in the detail schematics in Figure 7 through Figure 13.

Synchronizing circuits.--Inputs to the synchronizing section are timing pulses from the digital computer. The output pulses of this section control the various sections of the converter. The principal parts of the synchronizing section of the converter are illustrated in the block diagram in Figure 6. The P_{30} pulse is amplified by the pulse amplifier identified as transistor TR17 on the schematic of Figure 7. The output pulse from this amplifier is used to reset the two flip-flops contained in the digital Output Section and the flip-flop contained in the Synchronizing Section.

Analog threshold detectors.--This section of the converter analyzes the information from the Analog Program. The absolute value of the error voltage is applied to the Bit Information input of the Bit Threshold Detector. The schematic of the Threshold Detectors is illustrated in Figure 8. When the magnitude of this error exceeds a preset value in coincidence with an interrogation pulse from the Synchronizing Section, a pulse is produced at the output of the detector. A similar detector is used for an analog input that is non-zero for one polarity of the error voltage only. The output of this detector contains the sign information of the error

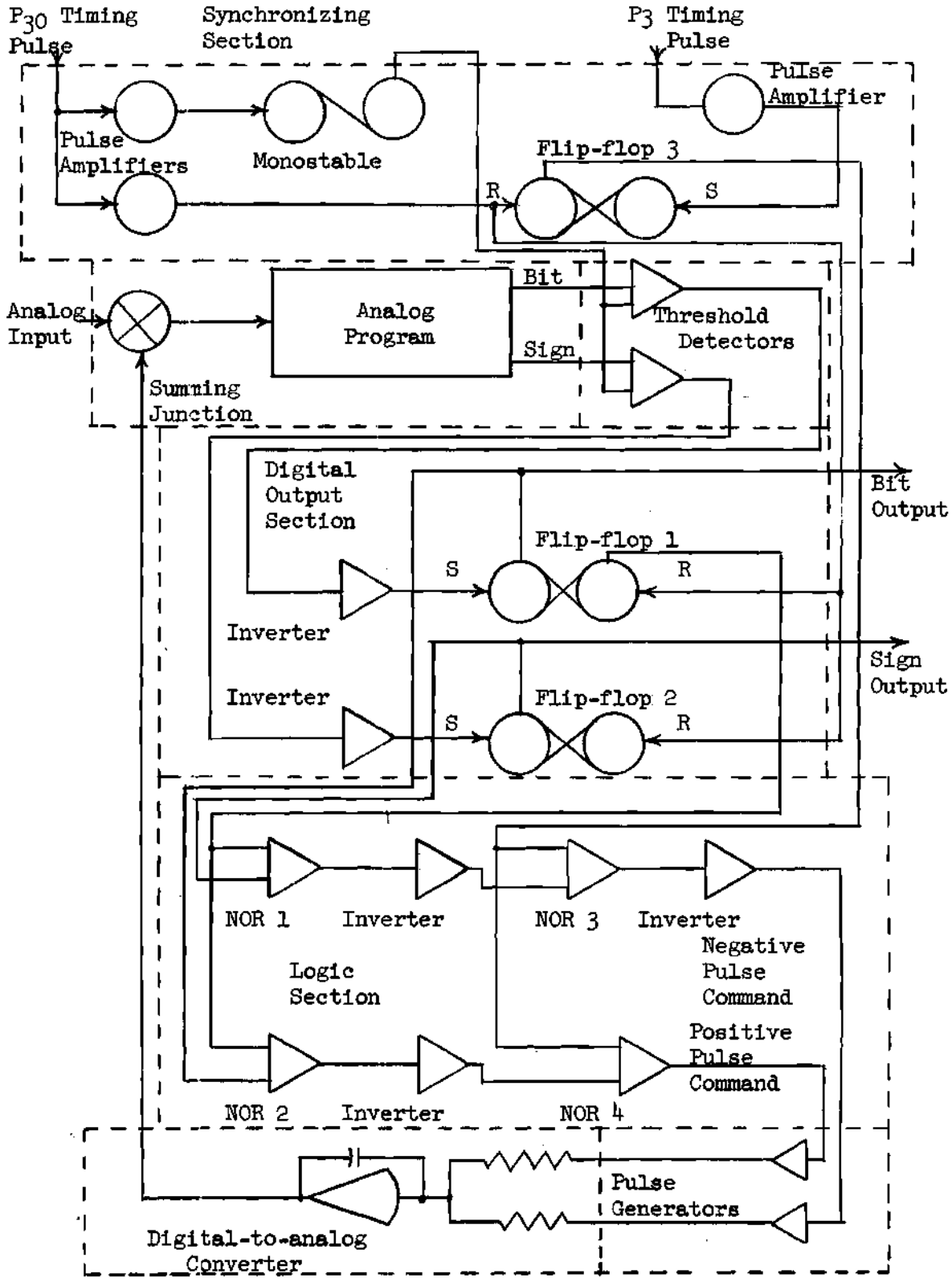


Figure 6. Block Diagram of the Analog-to-digital Converter

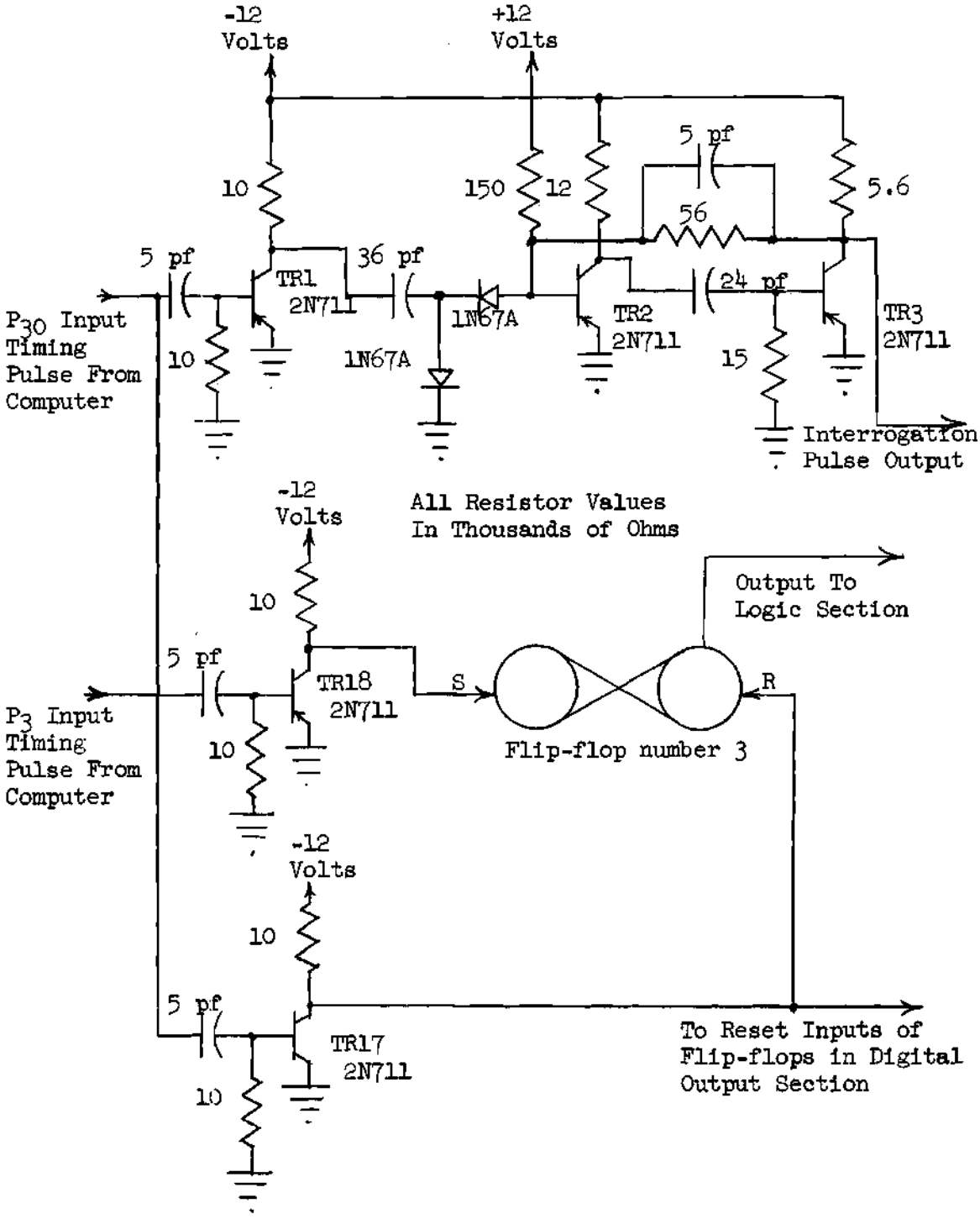


Figure 7. Detail Schematic of Synchronizing Section

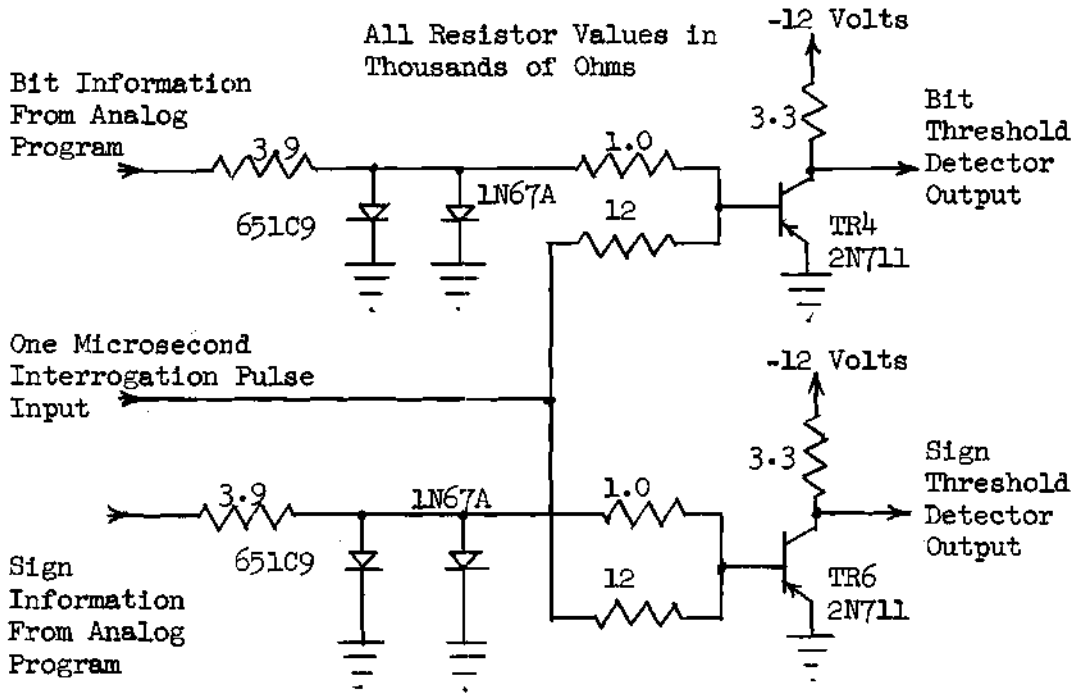


Figure 8. Detail Schematic of Analog Threshold Detectors

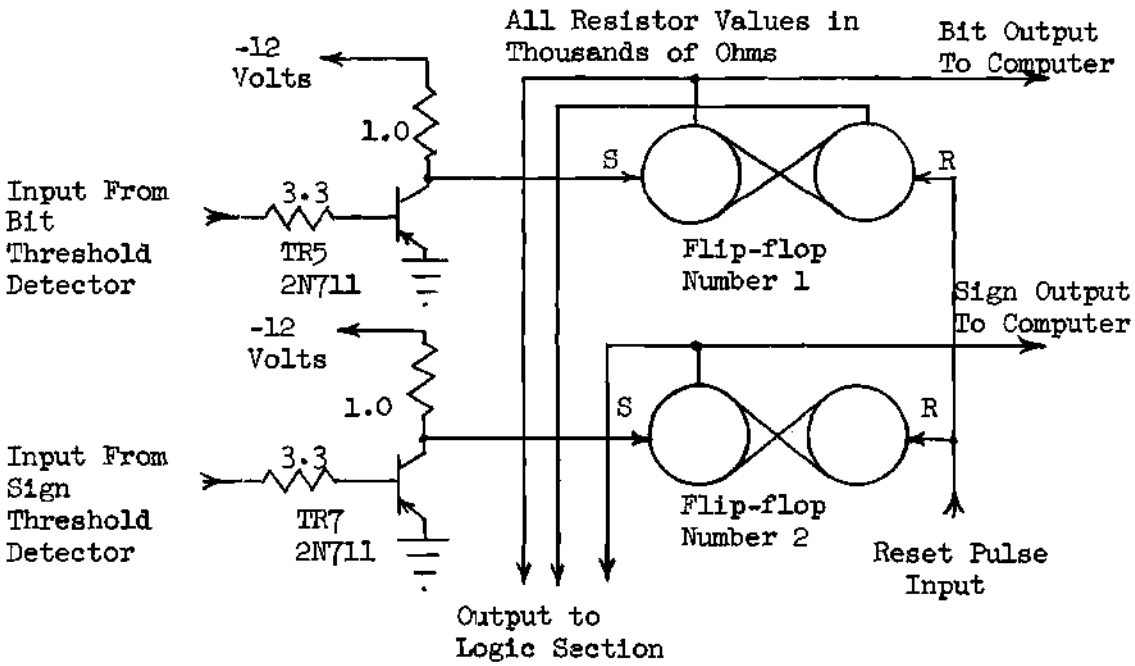


Figure 9. Detail Schematic of Digital Output Section

voltage. The presence of pulses at the outputs of these detectors indicate that the error voltage has exceeded the threshold level in coincidence with the interrogation pulse. The detector is a simple transistor switch with two inputs through resistors to a summing junction at the base of the transistor. One of the input signals to each detector is the interrogation pulse. This input has two possible voltage levels. A negative voltage exists during the period between the interrogation pulses. In the one microsecond interval of the interrogation pulse, the voltage at this point is at zero volts. When the analog input to the detector is positive with respect to the threshold level at the time of the interrogation pulse, the output of the detector changes state producing a pulse one microsecond wide at its output.

A diode network is provided at the analog input to each of the detectors to limit the voltage applied to the detector. This protects the transistors from high voltages that might be generated at the output of the Analog Program. This network uses a silicon zener diode to limit the input at about minus five volts and a germanium diode to limit the input at about plus 0.3 volts.

Digital output.--The digital output section of the converter is composed of two identical circuits. These two circuits present the information from the pulses at the output of the Threshold Detectors during the period that it will be accepted by the digital computer. This period is the time between the interrogation pulse and the next P_{30} pulse.

The output pulses of the Threshold Detectors are amplified through pulse inverters and are applied to the set inputs of the output flip-flops. The output flip-flop circuits used are the Packard Bell digital

modules model TF4 which are compatible with the input circuits to the TRICE computer. These inverting pulse amplifiers are transistors TR5 and TR7 in Figure 9. The output flip-flops are number one and number two in Figure 9. The presence of a negative eight volts at the output of the bit flip-flop indicates that the direction of the change in the analog input that is indicated by the output condition of the bit flip-flop was in the negative direction. An output of zero volts in the sign flip-flop at this time would indicate that the change was in the positive direction. When the value of the bit output is zero volts, the information from the sign output is ignored by the digital computer.

Logic section.--The Logic Section of the converter performs two tasks. The first is to examine the two digital outputs and detect both the presence of an output bit and the sign of this bit. Two NOR circuits are included for this function. These are number one and number two on the block diagram and are transistors TR8 and TR13 on Figure 10. If the error voltage exceeds a magnitude equal to one bit, the Threshold Detectors produce a pulse to set the output flip-flops. An output is produced simultaneously at the output of one of these NOR circuits depending on the sign of the error voltage. The information produced at this point is identical to that at the output of the Threshold Detectors but exists for the period between the interrogation pulse and the next P_{30} pulse.

The second task for the logic section is to produce a command pulse on one of two outputs during the period between the P_3 pulse and the P_{30} pulse if there was a pulse at the corresponding output of NOR circuits number one or number two. This command pulse has an accurate width and is used to control the Pulse Generator gates. A comparison is made

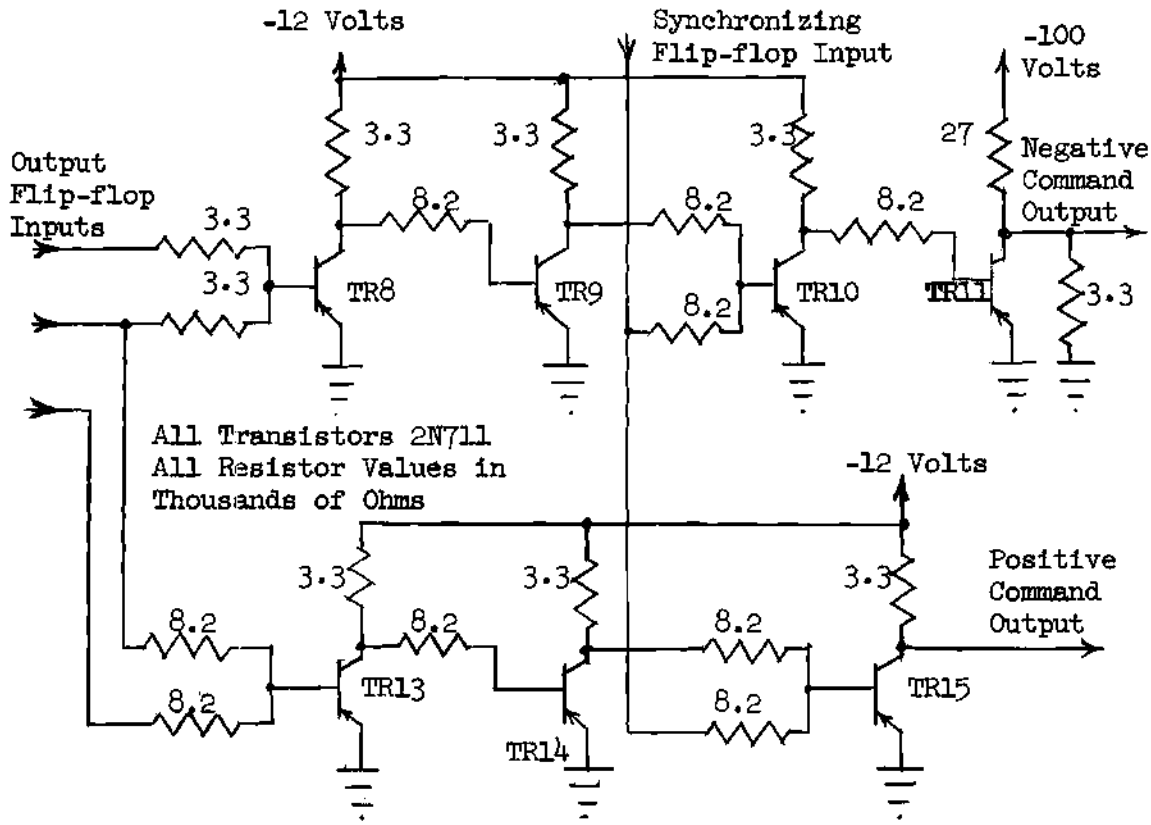


Figure 10. Detail Schematic of Logic Section

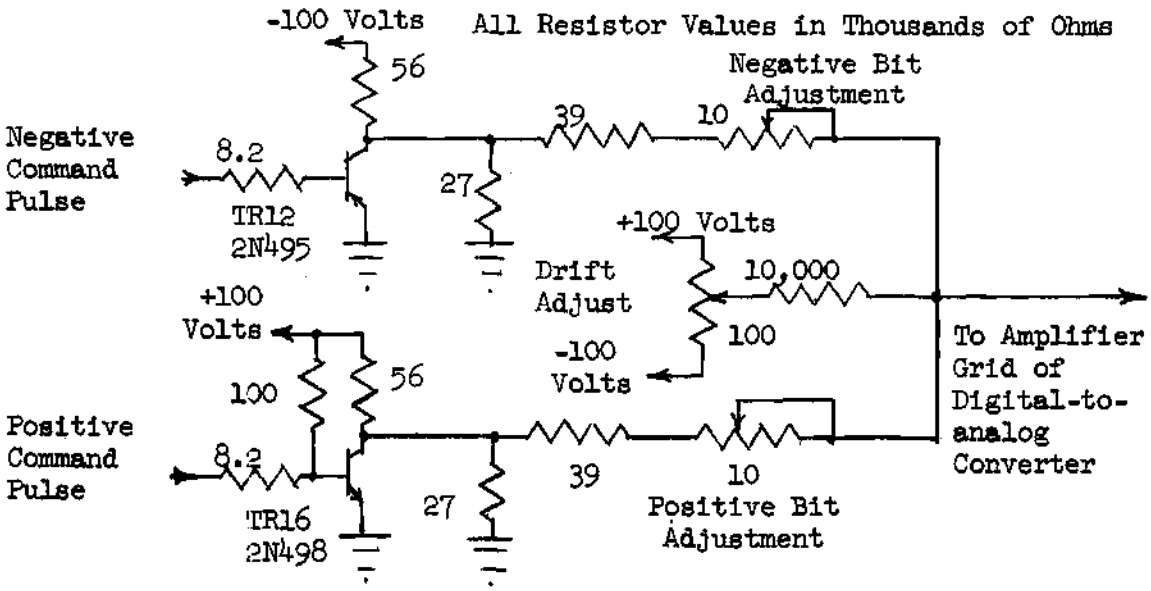


Figure 11. Detail Schematic of Pulse Generators

between the outputs of NOR circuits one and two and the output of the flip-flop contained in the Synchronizing Section. These pulses which are accurately controlled in duration are used to open the gates in the Pulse Generator which in turn generates a negative or positive pulse to feed into the digital-to-analog converter.

Pulse generators.--The Pulse Generator section contains two complementary transistor switches that are controlled by the Logic Section. When a command pulse is applied to the transistor gate, a regulated amplitude pulse is applied to the input of the digital-to-analog converter for the duration of the command pulse. These gates are identified as transistors TR12 and TR16 in Figure 11.

Digital-to-analog converter.--The digital-to-analog converter consists of the operational amplifier with a capacitor as the feedback element as described in a previous section of this chapter. A summing resistor is supplied to each output of the Pulse Generator to accept the positive and negative pulses into the integrator. This integrator circuit is shown in the complete diagram of the converter in Figure 6. The input resistors to this integrator are shown in detail in the schematic of the Pulse Generators in Figure 11. They include the resistive voltage divider in the collector circuit of the transistor gates and the series resistors to the common grid connection. The variable resistors are included to allow a fine adjustment of the positive and negative pulses.

Analog program.--The detailed analog program used in the converter is shown in Figure 12. The digital-to-analog converter includes Amplifier 1. Amplifier 2 provides a constant gain for the error voltage. Amplifiers 3 and 4 comprise a modified V-circuit or absolute-value circuit. The outputs of these last two amplifiers are the analog input information for

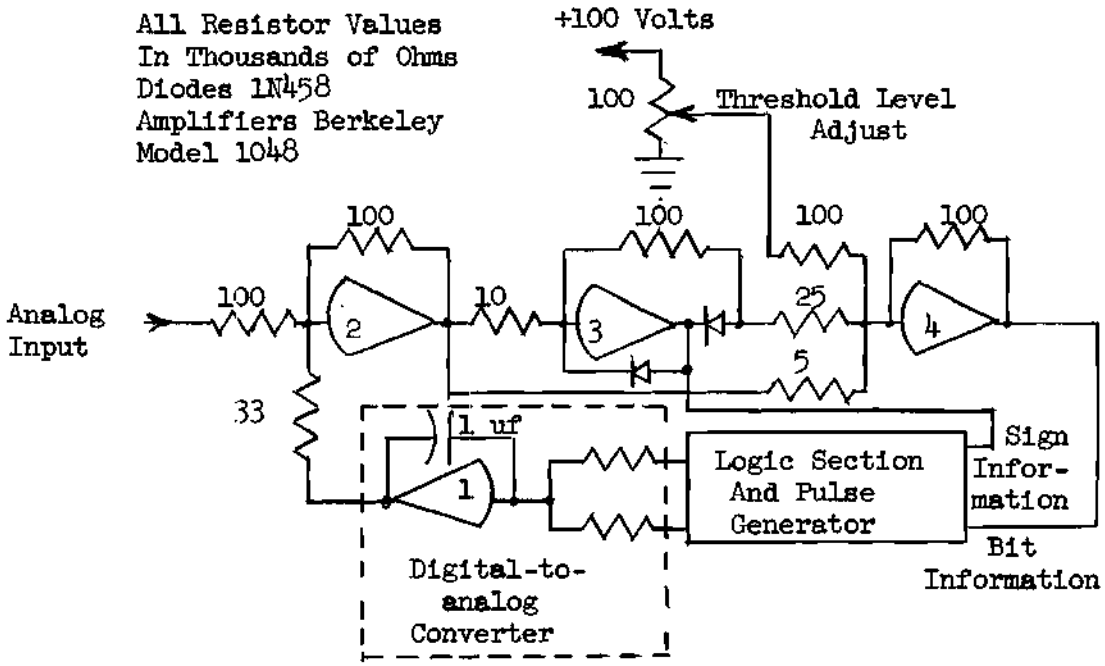


Figure 12. Detail Analog Program Used In Analog-to-digital Converter

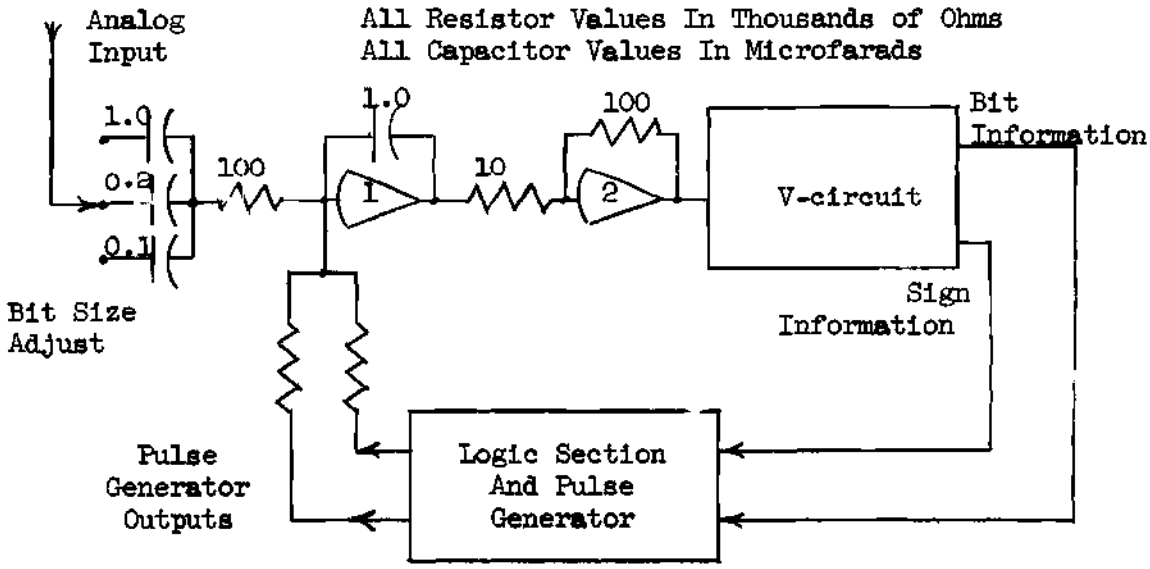


Figure 13. Modified Analog Program Used In Analog-to-digital Converter

the Threshold Detectors.

The modified absolute-value circuit is only slightly different from conventional circuits used for this purpose in analog computation. The output of Amplifier 3 is limited to negative voltages only because of the diode connected around the amplifier. Negative input voltages that cause the output of Amplifier 3 to clamp to zero are reproduced at the output of Amplifier 4 with opposite polarity. Positive input voltages to Amplifier 3 are reproduced with a negative polarity at the output of this amplifier. The input to Amplifier 4 from the output of Amplifier 3 is given a gain of two over the other input. The resulting sum of the voltages at Amplifier 4 produces the same output polarity as before. This is due to twice the input value being subtracted from the input to Amplifier 4 for this unclamped case of Amplifier 3. An offset to Amplifier 4 is added as a modification to allow the adjustment of the threshold value of the Threshold Detector.

A modification to the Analog Program is shown in Figure 13 where the summing junction of the unknown input voltage and the feedback voltage in the converter is moved to the grid of the digital-to-analog converter. This requires that the analog voltage be differentiated before being summed with the pulses from the Pulse Generator. This modification was made to keep the output of all of the operational amplifiers within the same operating range to eliminate the possible effects of nonlinearities in the conversions.

CHAPTER IV

TEST AND EVALUATION

Objectives.--The performance of the analog-to-digital converter must be measured in order to evaluate the conversion technique developed in this study. The converter which was constructed and evaluated is a laboratory model built to determine the feasibility of the conversion technique used. With this consideration in mind, the performance tests of the converter do not evaluate the long term drift and long term bit-size stability. The short term stability of the converter operating under laboratory conditions is sufficiently good to allow measurements of performance to be made over periods of a half hour or more without adjustments being made on the converter. The test data collected on the laboratory model indicates that adequate long term stability can be achieved by careful design and control of the environment.

The primary restraint on the performance of the converter is the degree of accuracy and repeatability of the conversions. The first objective of the tests performed on the converter is to demonstrate the repeatability of the conversions. The conversion accuracy should be considered no better than the repeatability. If the repeatability meets the specifications, it is then necessary to show that the bit size may be adjusted to the desired value with sufficient accuracy. With the accuracy of the adjustment known, the repeatability will determine the overall conversion accuracy.

Test description.--The conversion accuracy and repeatability of the

analog-to-digital converter may be found from the converted digital values of accurately known input voltages. The nature of the system described in this thesis makes the most convenient test the measurement of an input voltage that changes between two well known values. If the rate of change of the input voltage is within the limits of the converter, the error voltage in the converter will be restricted to a limited range. This makes the converter insensitive to the magnitude of the voltage existing at its input with the exception of the differentiating capacitor at the input of the digital-to-analog converter. If this is a quality capacitor so that there is no appreciable change in capacitance with voltage, then there is no source of nonlinearity present in the converter.

A desirable test for the converter is the conversion of a precisely known input voltage change. The rate of change of this input voltage must not exceed the limit of the converter in order to prevent overloading. This input may be realized by passing a voltage step through a lowpass filter with the proper cutoff frequency. The lowpass filter used in this thesis has an exponential step response with the maximum slope determined by the magnitude of the step and the time constant of the lowpass filter. The exponential output of the filter will be within 0.1 percent of its final value after seven time constants and within 0.01 percent after ten time constants.

The general purpose analog computer usually contains a highly regulated positive and negative voltage source refered to as the computer reference. It is from this reference voltage source that problem variables such as initial conditions and bias voltages are obtained. The analog computer accuracy and repeatability depend upon this reference source

if the problem being considered derives such constants as initial conditions from it. Errors in the absolute value of the computer variables due to errors in the reference voltage may be compensated for by measuring them in terms of this reference voltage. For this reason and the fact that the reset pulse height is derived from this source, the measurements and evaluations of this converter consider this reference source as a standard. The reference voltages available for this test are plus 100 volts and minus 100 volts. These voltages are used to generate the step input to the lowpass filter by switching the input of the filter between them and signal ground. They are also used as the source for a null comparison of the exponential output voltage of the filter to insure that it has reached (sensibly) its final value before recording the digital output of the converter.

Instrumentation.--A block diagram of the instrumentation used in the test is illustrated in Figure 14. A step voltage was generated at the input of the lowpass filter by means of the snap action switch that connected the filter to either the reference voltage or to signal ground. The filter was built around an operational amplifier so that the input to the converter would have a very low source impedance. The parallel resistor and capacitor as the feedback element of the amplifier gives the amplifier the characteristics of a single section R-C lowpass filter. The time constant of the filter network was determined by the product of the resistance and capacitance in the feedback network. The output of the filter including the operational amplifier differs from the simple R-C filter by the inversion in the output voltage introduced by the operational amplifier.

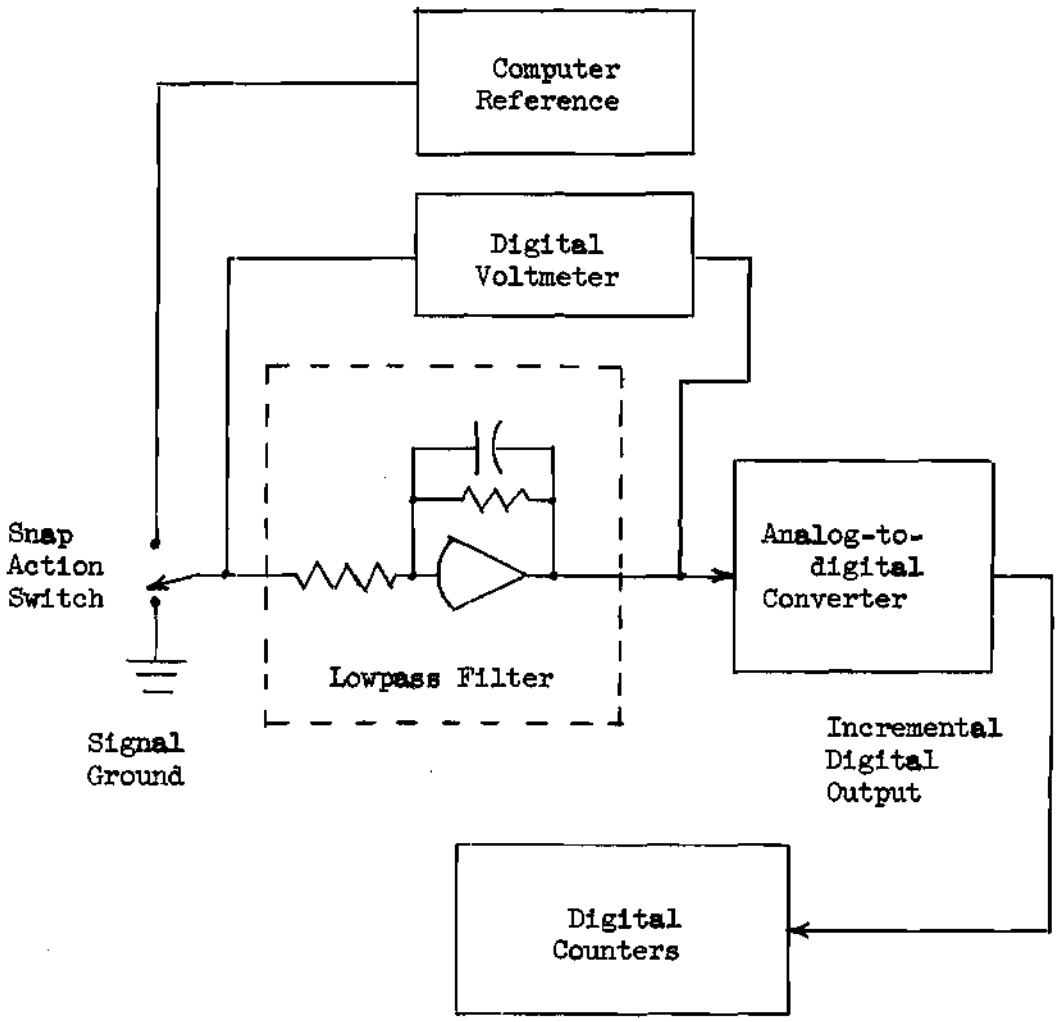


Figure 14. Diagram of Test Instrumentation

An Epsco digital voltmeter model DV-803 was used as the null detector for the input voltage to the converter. This voltage was compared to the computer reference voltage to accurately determine the value of the input at the start and finish of the exponential change. The maximum resolution of this digital voltmeter is one millivolt. This allowed the input voltage to the converter to be known with an accuracy of 0.001 percent refered to the reference supply which is better than the requirements of 0.1 percent for the repeatability and accuracy of the conversions.

The output of the analog-to-digital converter was monitored during the test by means of two digital counters. One counter totaled the positive pulses at the input of the digital-to-analog converter and the other counter totaled the negative pulses. The value of the input voltage to the converter was represented by the difference of the numbers contained in the counters.

Results.--The exponential waveform described above was applied to the input of the converter with sufficient time allowed in each condition of the amplifier input to insure that the output was within less than one bit of the final value. The bit size was calibrated to 50 millivolts by this waveform with respect to the computer reference supply for a conversion rate of approximately 15,000 bits per second which was used for these measurements. This value was chosen as a typical value for the converter. The input to the converter was cycled between signal ground and the 100 volt reference for several runs with each including four or more cycles. The total positive and negative bits for each cycle were recorded. This recorded digital value represents the converted value of the voltage change at the input of the converter. For this bit size, 2000 bits

represents a change of 100 volts. Larger voltage steps were made by cycling the filter input between plus 100 volts and minus 100 volts. The data from these test runs is tabulated in Table 2 and Table 3.

Conclusion.--The condensed results of all of the tests are given in Table 1. The largest deviation occurring in the bits recorded for input voltage change is listed for each run. The deviation in percent of total bits change is a measure of the repeatability of the converter. From Table 1 it is seen that the repeatability is better than 0.1 percent of full scale for all runs except Case H. The data tabulated was taken over a period of several hours with no adjustment made to the bit size in Case E through Case I after the bit size was calibrated in Case E. It is seen that there is a long term variation in the bit size but the short term stability is within 0.1 percent of the full scale range of the converter.

The short term repeatability, accuracy, and stability are sufficiently good to allow conversions to be made with errors no greater than 0.1 percent of the full scale range of the converter. The source of some of these errors and the suggested correction will be covered in Chapter V.

Table 1. Condensed Test Results

Case	Data Range Positive	Data Range Negative	Input Change (Volts)	Percent Deviation During Run Positive	Percent Deviation During Run Negative
A	4001 to 4003	4001 to 4003	200	0.05	0.05
B	4002 to 4004	4004 to 4005	200	0.05	0.025
C	4001 to 4003	4004 to 4005	200	0.05	0.025
D	4003 to 4005	4006 to 4008	200	0.05	0.05
E	1999	2001	100	0	0
F	2000	2001 to 2002	100	0	0.05
G	2000 to 2001	2001 to 2002	100	0.05	0.05
H	1999 to 2000	2001 to 2004	100	0.05	0.15
I	2002 to 2003	2004	100	0.05	0

Table 2. Tabulated Test Results

Case	Positive Steps (bits)	Negative Step (bits)	Input Change (volts)	Data Range Positive	Data Range Negative	Percent During Run Positive	Percent During Run Negative
A	4003	4002	200	4001	4001	0.05	0.05
	4002	4003	200	to	to		
	4001	4002	200	4003	4003		
	4001	4002	200				
	4003	4002	200	2 bits	2 bits		
	4002	4002	200				
	4003	4002	200				
	4002	4002	200				
	4003	4002	200				
	4001	4001	200				
	4001	4001	200				
B	4004	4004	200	4002	4004	0.05	0.025
	4003	4004	200	to	to		
	4002	4004	200	4004	4005		
	4002	4004	200				
	4002	4005	200	2 bits	1 bit		
	4003	4005	200				
C	4002	4005	200	4001	4004	0.05	0.025
	4002	4005	200	to	to		
	4003	4005	200	4003	4005		
	4002	4004	200				
	4001	4004	200	2 bits	1 bit		
	4003	4005	200				
	4001	4004	200				
D	4003	4007	200	4003	4006	0.05	0.05
	4005	4007	200	to	to		
	4005	4006	200	4005	4008		
	4005	4008	200				
	4004	4008	200	2 bits	2 bits		
	4004	4008	200				

Table 3. Tabulated Test Results

Case	Positive Steps (bits)	Negative Steps (bits	Input Change (volts)	Data Range Positive	Data Range Negative	Percent During Run Positive	Percent During Run Negative
E	1999	2001	100	0 bits	0 bits	0	0
	1999	2001	100				
	1999	2001	100				
	1999	2001	100				
	1999	2001	100				
F	2000	2002	100	0 bits	2001	0	0.05
	2000	2001	100		to		
	2000	2001	100		2002		
	2000	2001	100		1 bit		
G	2001	2001	100	2000	2001	0.05	0.05
	2000	2001	100	to	to		
	2000	2001	100	2001	2002		
	2000	2001	100				
	2000	2001	100	1 bit	1 bit		
	2000	2001	100				
	2000	2001	100				
	2000	2001	100				
	2000	2001	100				
	2000	2001	100				
	2000	2002	100				
H	1999	2001	100	1999	2001	0.05	0.15
	2000	2001	100	to	to		
	1999	2001	100	2000	2004		
	2000	2001	100				
	2000	2001	100	1 bit	3 bits		
	2000	2003	100				
	1999	2002	100				
	1999	2002	100				
	1999	2002	100				
	1999	2002	100				
	2000	2002	100				
	1999	2002	100				
	1999	2003	100				
	2000	2002	100				
	1999	2004	100				
I	2003	2004	100	2002	0 bits	0.05	0
	2003	2004	100	to			
	2003	2004	100	2003			
	2003	2004	100				
	2003	2004	100	1 bit			
	2003	2004	100				
	2002	2004	100				
	2002	2004	100				

CHAPTER V

SUMMARY AND CONCLUSIONS

Major parameters.--The incremental analog-to-digital converter developed in this thesis covers an input voltage range of plus 100 volts to minus 100 volts. The bit size was made adjustable over the range of 100 millivolts to 10 millivolts. The optimum conversion rate with respect to drift and conversion speed was found to be approximately 15,000 bits per second. The performance of the converter was measured for these values of bit size and bit rate and found to be equal to or better than 0.1 percent of full scale in accuracy and repeatability of the conversions. The approach to the problem of analog-to-digital conversion developed in this thesis has proven to be an acceptable method of conversion and has met all of the requirements except the maximum conversion rate of 100,000 bits per second. This does not impair the operation of the converter for the intended application but limits the maximum frequency of the input voltages.

Bandwidth.--The inputs to the analog-to-digital converter will be time varying voltages such as problem variables from a general-purpose analog computer. It is necessary to define the bandwidth of the converter in order to insure that these input voltages do not exceed the frequency limits of the system. Exceeding these limits may introduce errors in the converted values.

The lower frequency limit of the converter will be the frequency at which the drift of the converter causes appreciable error in the conversions. The lower frequency limit may be considered zero since

the average period of operation will usually be small compared to the time necessary to accumulate appreciable error from the drift sources.

The conversion rate of one bit per timing pulse defines the maximum rate of change of the digital output of the converter. This limit may be expressed as a frequency by defining an input voltage to the converter to be a sine wave with a peak value of 100 volts. The maximum rate of change of this input occurs when it has a value of zero volts. This value of maximum slope can be expressed as

$$\frac{dE}{dt} = 628 \text{ X (frequency of sine wave)}.$$

The maximum frequency of the input sine wave may be computed for a given bit size and bit rate. For the maximum bit size of 0.1 volts and the conversion rate used in Chapter IV of 15,000 bits per second, the maximum rate of change in the input voltage of the converter is 1,500 volts per second. This corresponds to a maximum frequency of 2.4 cycles per second. The maximum frequency limit for the input voltage in terms of the bit size in volts and the bit rate of the converter in cycles per second can be expressed as

$$\text{Maximum conversion frequency} = \frac{\text{(bit size) (bit rate)}}{628}.$$

This equation is based on the previously defined sine wave with a peak value equal to the full scale range of the converter.

This definition of the bandwidth of the converter is intended to give an approximation of the allowable range of input frequencies. It is

evident that sine waves with frequencies greater than the limit established above may be converted without error by reducing their peak values. The smaller the magnitude of the sine wave, the higher the maximum frequency limit. Exceeding the maximum rate of change that the converter is capable of causes the error voltage to increase beyond the threshold level of the Threshold Detectors. If this error voltage does not exceed the capabilities of the operational amplifiers, there will be only a delay before the digital output of the converter will reach the correct value. This delay for frequency components above the maximum frequency limit defined for the converter may be compared to the phase shift of a lowpass filter.

Relation of bit size to drift.--An inherent source of drift in the converter is in the integration circuit used for the digital-to-analog converter. This drift is related to the characteristics of the operational amplifier used in this circuit. This drift is frequently given in the specifications of the operational amplifier for an integrator configuration with a gain of unity. Increasing the gain of the integrator causes the drift to increase proportionally within limits. For a given pulse height and pulse width at the incremental digital input to the integrator, the gain of the integrator determines the bit size at the output of this amplifier. This gain must be made sufficiently large to insure a reasonable signal-to-noise ratio in the error voltage. The relationship of the bit size at the output of the digital-to-analog converter to the input voltage may be adjusted by scaling the input voltage with the appropriate constant. It is apparent that an increase in the bit size at the output of the integrator would cause an increase in the drift of this circuit due to the corresponding increase in gain. This drift introduces errors in the conversions.

The optimum bit size at the output of this amplifier was found experimentally to be approximately 100 millivolts for the operational amplifiers used.

Sources of conversion error.--There are three sources of error that should be considered in an effort to improve the performance of the converter. The major source of error occurs in the drift that may be attributed to the change in the offset voltage of the transistor switches due to temperature changes in these gates used for the Pulse Generators. This source of drift may be eliminated or reduced by keeping these transistors at a constant temperature. This may be done by increasing the thermal inertia of the transistors and by placing them in a controlled temperature environment. The first of these two methods was used in the unit discussed in this thesis. To obtain an additional decrease in drift and an increase in the stability of the bit size, all of the circuit elements shown in the detail schematic of the Pulse Generators in Figure 11 should be included in the controlled temperature environment.

A second source of error in the converter is in the regulation of the power supplies used. The area of concern is in the power to the operational amplifiers. The amplifier most sensitive to supply voltage changes in the Analog Program is the one used for the digital-to-analog converter. This is the point of lowest signal level and care should be taken to insure the highest possible degree of regulation in the voltages of the power supplies to this amplifier in order to reduce conversion errors.

A third source of error in the converter is in the noise voltage existing in the amplifiers of the Analog Program. The most critical

point in the program is in the digital-to-analog converter due to the low signal level at this point. Improvements may be made here by using an operational amplifier with the lowest noise level available.

Applications.--The primary application of the analog-to-digital converter is connecting a general purpose analog computer to the TRICE digital computer. The device may be used for other applications also. An application that is quite obvious is the operation as a digital-to-analog converter. This would allow the TRICE problem variables to be recorded on digital recorders by converting them to time varying voltages. This conversion would be accomplished by opening the feedback path and presenting the incremental digital value at the input of the Threshold Detectors in a two-bit binary parallel code. This information must be compatible with the input logic of the Threshold Detectors and must be present at these inputs at the time the one microsecond interrogation pulse occurs. Other applications include analog computational methods where it is important to know if a voltage has changed by a certain amount.

BIBLIOGRAPHY

Bowers, F. K., "What Use is Delta Modulation to the Transmission Engineer?" Transactions of the American Institute of Electrical Engineers, Vol. 78, 1957, pp. 142-147.

Burke, H. E., "A Survey on Analog-to-digital Converters," Proceedings of the Institute of Radio Engineers, Vol. 41, August 1953, pp. 1455-1462.

Jackson, Albert S., Analog Computation, New York, McGraw-Hill, 1960, pp. 559-573.

Smith, B. D., "Coding by Feedback Methods," Proceedings of the Institute of Radio Engineers, Vol. 41, August 1953, pp. 1053-1058.